conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

REMARKS

Claims 1-3, 10-11, and 17 have been amended. Claims 1-22 are currently pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Objections to the Drawings:

FIGS. 1-4 of the Drawings were objected to for failing to denote that only that which is old in the art is illustrated. The objection has been obviated by the amendments to the Drawings presented in the accompanying Request for Approval of Drawing Changes. For example, the addition of the designation "(Related Art)" obviates the objection to the Drawings under MPEP §608.02(g). The intent of MPEP §608.02(g) is to ensure that Drawings depicting unclaimed subject matter may be distinguished from Drawings depicting embodiments of the claimed invention. For example, MPEP §608.02(g) only requires the addition of a legend "such as 'Prior Art'." (Emphasis added.) Since the addition of the legend "(Related Art)" serves to distinguish those Figures representing unclaimed subject matter (e.g., FIGS. 1-4) from the other Figures in the application, the amendments to the Drawings satisfy MPEP §608.02(g). It is submitted that this objection has now been overcome.

Objections to the Claims:

Claims 2-8, 10-16, and 18-20 were objected to because the lines are too closely together. A copy of all claims in the case, incorporating all amendments, with lines one and one-half spaced on good quality paper as required under 37 CFR 1.52(b) is included in Attachment A. Therefore, removal of the objections to claims 2-8, 10-16, and 18-20 is respectfully requested.

Section 112, 2nd Paragraph, Rejections:

Claims 1, 2, 3, 7, 10, 11, 15, and 17 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. Claims 1, 2, 3, 10, 11, and 17 have been amended. These amendments are believed to clarify the claim language in a manner that addresses the concerns about those claims expressed in the Office Action.

Claims 2 and 10 have been amended for consistency with accepted Markush claim practice (see MPEP § 2173.05(h)). As the Examiner will note from MPEP § 2173.05(h), claims 7 and 15 were filed in accordance with accepted Markush claim practice. Accordingly, removal of the § 112, second paragraph, rejection of claims 1, 2, 3, 7, 10, 11, 15, and 17 is respectfully requested.

Section 103 Rejections:

Claims 1-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,093,631 to Jaso et al. (hereinafter "Jaso") in view of pages 1-6 of Applicant's Specification and Figs. 1-4 of Applicant's Drawings. As set forth in more detail below, the rejections of claims 1-22 are respectfully traversed.

To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond,* 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

None of the cited art teaches or suggests etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches. Amended independent claim 1 recites in part: "[a] method, comprising: etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches." Independent claims 9 and 17 recite a similar limitation.

Jaso discloses a method and apparatus for planarizing damascene metallic circuit patterns. Jaso, however, does not teach or suggest etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches. As stated in the Office

Action, "Jaso et al. do not teach that the first trench is a relatively wide trench and the series of second trenches are relatively narrow trenches." (Office Action -- page 3). Therefore, Jaso cannot teach or suggest etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches, as recited in claim 1.

Pages 1-6 and Figs. 1-4 of Applicant's disclosure are not available as prior art against the claims in this case. When applicant states that something is prior art, it is taken as being available as prior art against the claims. Admitted prior art can be used in obviousness rejection. *In re Nomiya*, 509 F.2d 566, 184 USPQ 607, 610 (CCPA 1975). MPEP § 2129. Neither Applicant nor Applicant's representative has ever stated or "admitted" that pages 1-6 and Figs. 1-4 of Applicant's disclosure are prior art. The text on these pages and Figs. 1-4 were included in the Related Art section because Applicant did not intend to claim this subject matter. There is no evidence on record that pages 1-6 and Figs. 1-4 of Applicant's disclosure are actually prior art to the claims. Therefore, pages 1-6 and Figs. 1-4 of Applicant's disclosure cannot be used in an obviousness rejection against the claims in the case.

Hypothetically speaking, even if the text on pages 1-6 and Figs. 1-4 of Applicant's disclosure were contained in a document that is available as prior art against the claims in this case, the text on pages 1-6 and Figs. 1-4 cannot be properly considered as prior art. For example, as stated in the Specification, "FIGS. 2-4 illustrate a typical damascene process and the localized thinning or "dishing" problem experienced by conventional metal CMP processes." (Specification -- page 3, lines 17-19). Therefore, pages 1-6 and Figs. 1-4 of Applicant's disclosure present a problem with metal CMP processes (i.e., localized thinning or dishing). This disclosure of the problem in pages 1-6 and Figs. 1-4, however, does not constitute a "nonpreferred embodiment" of the disclosure that may be properly considered as prior art. An example of a non-preferred embodiment may be an "unattractive" method of etching dummy trenches or an "unattractive" spacing of dummy trenches. In contrast, dummy trenches are not even mentioned in the "Description of the Related Art" on pages 1-6 or illustrated in Figs. 1-4 of Applicant's disclosure.

Assuming, for the sake of argument, that pages 1-6 and Figs. 1-4 of Applicant's disclosure are available as prior art against the claims, pages 1-6 and Figs. 1-4 of Applicant's disclosure do not disclose etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches, as recited in claim 1. Therefore, since neither Jaso nor pages 1-6 and Figs. 1-4 of Applicant's disclosure teach or suggest all limitations of claim 1, the

combination of Jaso and pages 1-6 and Figs. 1-4 of Applicant's disclosure also does not teach or suggest all limitations of claim 1.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). MPEP 2143.01.

Even if the cited art can be modified, as suggested by the Office Action, the resultant modifications are not obvious because the prior art does not suggest the desirability of the modifications. For example, Jaso states that "it is one aspect of the invention to decrease the difference in pattern factor across the chip surface by providing a uniform metal density (pattern factor) across the surface of the chip and, concomitantly, of the wafer." (Jaso -- col. 3, lines 34-37). In addition, Jaso states that "the pattern factor for a particular area or region may be defined as the area covered by the metal divided by the total area of the particular area or region." (Jaso -- col. 3, lines 7-10). Therefore, if the definition of pattern factor disclosed by Jaso is applied to Figs. 2-4 of Applicant's disclosure, then a pattern factor for a first area containing narrow trenches 22 and a second area containing wide trench 24 would be approximately the same according to Jaso. Jaso also states that "to overcome the dishing effect and other non-planarization, the invention decreases the differences in pattern factors for regions on the chip." (Jaso -- col. 3, lines 29-31). Jaso further states that "in another preferred aspect of the invention, the lower pattern factor design limit can be artificially generated for any given region on the chip or wafer surface by using a dummy circuit design." (Jaso -- col. 3, lines 57-60). As such, Jaso teaches that because the two areas of Figs. 2-4 of Applicant's disclosure have approximately equal pattern factors, these areas would not suffer from the dishing effect and other non-planarization. Consequently, Jaso teaches that there would be no need for including a dummy circuit design in either area of Figs. 2-4. Jaso, therefore, does not teach, suggest the desirability of, or provide motivation for including the dummy circuit design of Jaso in the semiconductor topography illustrated in Figs. 2-4 of Applicant's disclosure. In addition, pages 1-6 and Figs. 1-4 of Applicant's disclosure do not teach, suggest the desirability of, or provide motivation for including the dummy circuit design of Jaso in either area of the semiconductor topography illustrated in Figs. 2-4. Therefore, none of the cited art, alone or in combination, suggests the desirability of the modifications proposed in the Office Action. As such, the modifications proposed by the Office Action are not obvious.

For at least the reasons stated above, none of the cited art teaches or suggests the limitations of claims 1, 9, and 17. Therefore, claims 1, 9, and 17, and claims dependent therefrom, are patentably

distinct over the cited art. Accordingly, removal of the § 103(a) rejections of claims 1-22 is respectfully requested.

NOTICE OF CHANGE OF ATTORNEY DOCKET NUMBER

The Commissioner is requested to change the attorney docket number for the above-identified patent application as set forth below.

Old Number:	5298-02501
New Number:	5298-02502

CONCLUSION

In this response, claims 1-3, 10-11, and 17 have been amended. Rejections of claims 1-22 have been addressed. Therefore, this response constitutes a complete response to all of the issues raised in the Office Action mailed July 3, 2002. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-22 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

The Commissioner is authorized to charge any required fees or credit any overpayment to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5298-02502.

Respectfully submitted,

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AMM

ATTACHMENT A
"Marked-Up" Amendments

IN THE CLAIMS:

Please amend claims 1-3, 10-11, and 17 as follows:

1. (Twice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material;

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide [trenches] trench, wherein said dummy conductors are electrically separate from [of] electrically conductive features of an ensuing integrated circuit.

2. (Amended) The method of claim 1, wherein said conductive material comprises a metal selected from [said] the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. (Amended) The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said [wide and] series of relatively narrow trenches and said relatively wide trench.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. The method of claim 1, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to the upper surface.

6. The method of claim 5, wherein said polishing comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said conductive material.

7. The method of claim 5, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

9. A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

10. (Amended) The method of claim 9, wherein said conductive material comprises a metal selected from [said] the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said [wide and narrow] said trench and said series of trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. The method of claim 9, wherein said polishing comprises applying an abrasive polishing surface to an upper surface of said conductive material while moving the abrasive polishing surface relative to said upper surface.

14. The method of claim 13, wherein said polishing further comprises applying a liquid substantially free of particulate matter between said abrasive polishing surface and said upper surface of said conductive material.

15. The method of claim 13, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. The method of claim 9, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

17. (Twice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said <u>series of relatively</u> narrow [and wide] trenches <u>and said relatively wide trench</u>, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

21. The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.